Remark

Applicant respectfully requests reconsideration of this application as amended. Claims 2 & 25-28 haven been canceled, and claims 31-33 have been added. Therefore, claims 1, 3-24, 29-30, and 31-33 are now presented for examination.

35 U.S.C. §102 Rejection,

In the final office action mailed 4/07/00, the Examiner rejected claims 1,2,16,21,22 & 25-30 under 35 USC 102(e) as being anticipated by Gates.

These claims have been amended to traverse Gates. In particular, all of the pending claims require that the instruction memory be capable of storing more than a single bus transaction. This is in contrast to Gates which teaches a command register configured to hold only a single command, wherein the single command is utilized to generate a parity error on a PCI bus.

In general, embodiments of the claimed invention relate to a bus transaction generator that can drive multiple signals corresponding to bus transactions onto a computer bus. According to some embodiments, the transaction generator may drive onto the bus signals representing an exact sequence of bus transactions to determine the response of either other bus agents and/or the bus itself. In one embodiment, the user is able to load predefined instruction words into the instruction memory of the bus transaction generator to facilitate the generation of a controlled sequence of bus transactions.

In contrast, Gates describes an error generation circuit that simply drives at most a single command onto the bus and causes a incorrect parity value to be driven on the bus to create an error. The apparent purpose of the Gates teachings is test bus response to an error condition. As mentioned above, Gates discloses a command register capable of holding a single command. *See Abstract ("**an error command** is loaded into the command register"); and col. 2, lines 40-41 ("...a device on the PCI bus loads **an error command** into the command register of the bus error generation circuit of the integrated circuit via the PCI bus");* Nowhere in Gates is it suggested that multiple bus transactions, let alone commands be loaded into the command registry to facilitate driving signals corresponding to multiple bus transactions onto the bus. In fact, Gates teaches to completely clear the command register once the single command to generate the error is driven on the bus. *See col. 2, lines 59-62.*

Accordingly, the claimed embodiments are not anticipated by Gates under 35 USC 102, since the command register of Gates, capable of holding only a single command, is a distinctly different element from the instruction memory of claimed embodiments.

The Examiner also rejected claims 3,7 & 8 under 35 USC 103(a) over Gates. It is assertion of the applicant that Gates does not teach, suggest or motivate one to create an error generation circuit with a multiple command registry, so Gates would not in and of itself render claims 3, 7 & 8 obvious under 35 USC 10, let alone all of the other claims pending in this application. *See MPEP 706.02(j).* Gates actually teaches away from a registry capable of storing multiple commands. First, Gates teaches to clear the registry after the command is driven on the bus, therefore a registry that could hold more than one

command would be nonsensical, since the any command other than the first would be erased before being driven onto the bus. Second, Gates teaches that the bus error condition is generated in a clock cycle immediately after a bus transaction is performed on the bus, therefore it would not be obvious to drive additional bus transactions or commands onto the bus if the stated goal of causing an error condition has been achieved. Accordingly, the claimed embodiments are non-obvious with regard to the Gates reference alone.

For clarity, each of the elements that distinguish the claims over Gates are discussed below with regard to each claim or set of claims:

Claim 1 and Dependents 3-14 & 32-33:

As discussed above Gates does not anticipate, teach, suggest or motivate the claim 1 limitation; "instruction memory to store a plurality of predefined bus stimuli instructions, the predefined bus stimuli instructions representing a plurality of bus transactions."

Accordingly, these claims are in condition for allowance over Gates for at least this reason.

Claim 15:

As discussed above Gates does not anticipate, teach, suggest or motivate the claim 15 limitation; "an instruction memory for storing a predefined sequence of bus stimuli representing a plurality of bus transactions."

Accordingly, claim 15 is in a condition for allowance over Gates for at least this reason.

Claim 16 and Dependents 17-20:

As discussed above Gates does not anticipate, teach, suggest or motivate the claim 16 limitation; "a first means for storing instructions representing a plurality of predefined bus transactions."

Accordingly, claim 16 is in a condition for allowance over Gates for at least this reason.

Claim 21 and Dependents 22-24:

As discussed above Gates does not anticipate, teach, suggest or motivate the claim 21 limitation; "executing the plurality of bus transactions by converting the instruction words to signals and driving the signals on the bus." Gates only teaches to execute a single command in order to generate an error condition on the bus.

Accordingly, these claims are in a condition for allowance over Gates for at least this reason.

Claim 29 and Dependent 30:

As discussed above Gates does not anticipate, teach, suggest or motivate the claim 29 limitation; "an instruction memory to store a plurality of predefined bus stimuli instructions, the predefined bus stimuli instructions representing signals associated with a plurality of bus transactions on a bus."

Accordingly, these claims are in a condition for allowance over Gates for at least this reason.

Claim 31:

As discussed above, Gates does not anticipate the limitations from claim 31 of, "generating a plurality of instructions words corresponding to sequence of bus

transactions" and "storing the instructions words in a memory." Furthermore Gates does not anticipate, teach, suggest or motivate the limitation of, "executing the bus transactions by converting the plurality of instruction words into signals and driving the signals onto the bus in the predefined sequence." Gates teaches only to drive a single command onto the bus to generate an error condition.

Accordingly, this claim is in a condition for allowance over Gates for at least these reasons.

Conclusion

The undersigned respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, the undersigned respectfully requests the rejections be withdrawn and the claims as amended be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

The undersigned respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 8/22/00

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